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UTILITY PATENT APPLICATION TRANSMITTAL

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Attorney Docket No. 0756-2070

First Inventor or Application Identifier: Jun KOYAMA et al.

Title: REDUNDANCY SHIFT REGISTER CIRCUIT FOR DRIVER CIRCUIT IN ACTIVE MATRIX TYPE LIQUID CRYSTAL DISPLAY DEVICE

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jc710 U.S. PTO 11/24/99

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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original, and a duplicate for fee processing)
2. [X] Specification *Total Pages* [26]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) *Total Sheets* [11]
4. [X] Oath or Declaration *Total Pages* [2]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d))
      (for continuation/divisional with Box 17 completed)
      [Note Box 5 below]
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [X] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

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6. [ ] Microfiche Computer Program *(Appendix)*
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   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8 [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney
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10 [ ] English Translation Document *(if applicable)*
11 [X] Information Disclosure Statement [X] Copies of IDS Citations
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*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. **If a CONTINUING APPLICATION**, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
Divisional of prior application Serial No. 08/803,217 filed February 20, 1997; which itself is a Continuation of application Serial No. 08/427,096, filed April 21, 1995, now abandoned.
Prior application information: Examiner: P. Bell Group/Art Unit: 2775

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of	)
Jun KOYAMA et al.	)
Based On Serial No. 08/803,217	) Art Unit: 2775
Which Was Filed: February 20, 1997	) Examiner: P. Bell
For: REDUNDANCY SHIFT REGISTER	)
CIRCUIT FOR DRIVER CIRCUIT	)
IN ACTIVE MATRIX TYPE LIQUID	)
CRYSTAL DISPLAY DEVICE	) Date: November 24, 1999

<u>PRELIMINARY AMENDMENT</u>

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

<u>IN THE SPECIFICATION</u>:

Before the first sentence of the specification, insert --This application is a Divisional of Application Serial No. 08/803,217 filed February 20, 1997;

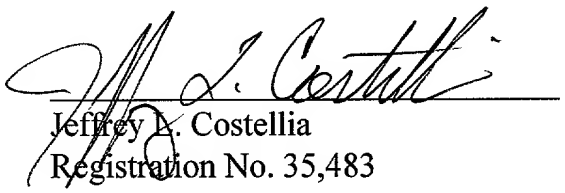
which itself is a Continuation of application Serial No. 08/427,096, filed April 21, 1995, now abandoned.--

REMARKS

This application has been amended to include the continuing application data thereof.

Examination on the merits is requested.

Respectfully submitted,



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REDUNDANCY SHIFT REGISTER CIRCUIT FOR DRIVER CIRCUIT IN ACTIVE MATRIX TYPE LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a shift register circuit constructed by thin film transistor (TFTs), in particular, a redundancy shift register circuit.

A shift register circuit in which TFTs are used is utilized in a driver circuit of an image sensor or a liquid crystal display (LCD) device, in particular, recently, in a driver circuit of an active matrix type display device.

In an active matrix type display device, each pixel is arranged in a cross section portion of an active matrix circuit and connected with a switching element, and image information is controlled by on/off of the switching element. As a display media of such display device, a liquid crystal, plasma, an object (state) capable of electrically changing an optical characteristic (reflectance, refractive index, transmimissivity, emission (luminous) strength) or the like are used. As a switching element, in particular, a three terminal element, that is, a field effect transistor having a gate, a source and a drain is used.

In a matrix circuit, a signal line (a gate line) which is arranged in parallel to a line is connected with gate electrodes of transistors with respect to the line, and a signal line (a source line) which is arranged in parallel to a column is connected with source (or drain) electrodes of the transistors with respect to the column. A circuit for driving the gate line is referred to as a gate driver circuit, and a circuit for driving the source line is referred to as a source driver circuit.

Since the gate driver circuit generates a vertical line scan timing signal with respect to an active matrix type display device, a shift register includes serial-connected

registers (in a single line) corresponding to the number of gate lines with a vertical direction. As a result, switching of thin film transistors (TFTs) in an active matrix type display device is performed by the gate driver circuit.

Since the source driver circuit generates a horizontal line image signal of image data to be displayed on an active matrix type display device, a shift register includes serial-connected registers (in a single line) corresponding to the number of source lines with a horizontal direction. Also, by a latch pulse synchronous with a horizontal scan signal, an analog switch is turned on or off. As a result, a current is supplied from the source driver circuit to TFTs in an active matrix type display device, to control alignment of a liquid crystal cell.

Referring to Fig.5, a common active matrix type display device will be described.

A horizontal line scan timing signal is generated by a shift register 51. Analog switches 53 and 54 are turned on and then a video signal is stored in analog memories 55 and 56 in response to the horizontal line scan timing signal. Image data corresponding to the video signal stored in the analog memories 55 and 56 is stored in analog memories 59 and 60 through analog switches 57 and 58 turned on by timing of a latch pulse. The image data is supplied from the analog buffers 59 and 60 to source lines of TFTs 63 and 64 through analog buffers 61 and 62 in an active matrix circuit 70 of an active matrix type liquid crystal display device in timing of the latch pulse.

On the other hand, a vertical line scan timing signal is generated by a shift register 52 and then supplied to gate lines of the TFTs 63 and 64 in the active matrix circuit 70 of the active matrix type liquid crystal display device. Therefore, the image data (voltage) supplied to the source lines is applied to liquid crystals 65 and 66, to determine alignment of the liquid crystals 65 and 66 connected with drain lines of the TFTs 63 and 64. the active matrix type liquid

crystal display device is operated by the above operation.

Generally, a shift register includes a circuit as shown in Figs.6A and 6B, in particular, a D-type flip-flop. Fig.6A shows a D-type flip-flop constructed using analog switches, and Fig.6B shows a D-type flip-flop constructed using clocked invertors. These operation will be described below.

In Fig.6A, when an operation clock CK is a high level (H) and an input signal DATA is a high level (H), a complementary type transmission gate a-1 is turned on and then the input signal DATA is input to a complementary type invertor circuit a-2. Therefore, an output of the complementary type invertor circuit a-2 becomes a low level (L). In this state, complementary type transmission gates a-4 and a-5 are in a turn off state.

When the operation clock CK is changed to a low level (L) while the input signal DATA is a high level (H), the complementary transmission gate a-1 becomes a turn off state, the complementary type transmission gates a-4 and a-5 become a turn on state. Therefore, an output of the complementary invertor circuit a-2 is held to a low level (L).

Also, since the complementary type transmission gate a-5 becomes a turn on state, an output of an complementary type invertor circuit a-6 becomes a high level (H). In this state, a complementary type transmission gate a-8 becomes a turn off state.

When the operation clock CK is changed to a high level (H) again, the complementary transmission gate a-5 becomes a turn off state and the complementary type transmission gate a-8 becomes a turn on state, so that a previous signal level is held. Therefore, an output of the complementary type invertor circuit a-6 can be held to an input signal DATA having a high level (H) in synchronous with an operation clock CK.

As a result, a D-type flip-flop can be constructed using transmission gates. Also, when an input signal DATA is a low

level (L), the above described operation is performed.

In Fig.6B, when the operation clock CK is a high level (H) and the input signal DATA is a high level (H), an output of a complementary clocked invertor circuit b-1 becomes a low level (L) and then an output of the complementary invertor circuit b-2 becomes a high level (H). In this state, complementary clocked invertor circuits b-3 and b-4 are in a turn off state.

When the operation clock CK is changed to a low level (L) while the input signal DATA is a high level (H), the complementary clocked invertor circuits b-3 and b-4 are turned on, so that an output of the complementary type invertor circuit b-2 is held to a high level (H). An output of the complementary invertor circuit b-5 becomes a high level (H). In this state, the complementary clocked invertor circuit b-6 is a turn off state.

When the operation clock CK is changed to a high level again, the complementary type clocked invertor circuit becomes a turn off state, and the complementary type clocked invertor circuit becomes a turn on state. Therefore, an output of the complementary type invertor circuit can be held to an input signal DATA having a high level (H) in synchronous with an operation clock CK.

As a result, a D-type flip-flop is constructed by clocked invertors. Also, when an input signal DATA is a low level (L), the above described operation is performed.

In a shift register circuit used in gate and source driving circuits of a common active matrix type display device, as shown in Figs.2A and 2B, registers having the same number as the number of gate lines (or source lines) are connected in serial. In a gate driver circuit as shown in Fig.2A, outputs of registers SR_i (i=1 to n) in a shift register circuit 120 are connected to gate lines 123 and 124 through invertor type buffer circuits 121 and 122. In a source driver circuit as shown in Fig.2B, outputs of registers SR_i (i=1 to N) in a shift

register circuit 125 are connected to control terminals of sampling transmission gates 128 and 129 through invertor type buffer circuits 126 and 127.

If at least one register has defect in the shift register circuit having serial-connected registers, image data and scan timing signals output from the defect register and later connected register are abnormal, an accuracy image cannot be obtained. This problem is due to a yield of a shift register.

SUMMARY OF THE INVENTION

The object of the present invention is to solve the above problems.

As shown in Fig.1, a shift register circuit 104 includes at least one register group 103 and a register selecting switch 102. the register group 103 includes register lines 101a, 101b, ..., and 101n having a plurality of serial-connected registers SRAi, SRBi, ..., and SRZi (i = 1 to n), respectively. The register line selecting switch 103 selects one of the register lines.

In this structure, one register line is used as a main register line, and the other register lines are used as a subregister line. When a plurality of register groups are arranged in a shift register circuit, the register groups are connected with each other in serial, to use as a shift register constructing gate and source driver circuits. Defect detection terminals 105a, 105b, ..., 105n are arranged with the register lines in the register group, respectively, so that whether or not each register line operates normally is detected. An output of a last register of each shift register line is connected with the register line selecting switch 103.

The register line selecting switch 103 has at least one bias circuit (as described later). A voltage is always applied to the bias circuit, switching operation by the bias circuit is performed by providing one bias.

When one of the register lines is selected by the register line selecting switch 103, register column selecting switches 106a, 106b, ..., 106n selects registers included in the selected one of the register lines, respectively. The number of register column selecting switches coincides with the number of registers included in each register line. Each register column selecting switch selects one of a plurality of input signals as an output signal. A signal for selecting the output signal is generated by using an output signal of the bias circuit.

When defect is detected by examining a main register line using a defect detection terminal, one of subregister lines is examined by another defect detection terminal. When defect is not detected, the register line selecting switch 102 selects the one of the subregister lines. Simultaneously, the register column selecting switches select the registers of the selected subregister lines.

As a result, redundancy is performed for register lines in a register group, so that a yield for a whole shift register circuit can be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 shows a redundancy shift register circuit in a driving circuit of an active matrix type display device according to an embodiment of the present invention;

Figs.2A and 2B show a shift register circuit in a driving circuit of a common active matrix type display device, respectively;

Fig.3 shows a shift register circuit of an embodiment;

Fig.4 shows a shift register selecting switch of the embodiment;

Fig.5 shows a schematic view of a common active matrix type display device;

Figs.6A and 6B show a common register, respectively.

Figs.7A and 7B show a priority encoder circuit and a multiplexer circuit, respectively.

Figs.8A to 8C show a bias circuit, respectively.

Figs.9A to 9C show a register constructed by p-channel transistors;

Figs.10A to 10F show a method for forming complementary invertor circuit;

Fig.11A and 11B show a shift register selecting circuit of the embodiment;

Fig.12 shows a truth table of a priority encoder circuit; and

Fig.13 shows a shift register selecting switch of another embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A thin film device (such as a complementary invertor circuit) used in the present invention will be described below.

A silicon oxide film having a thickness of 1000 to 3000 Å is formed as a base oxide film on a glass substrate (a low alkaline glass such as Corning 7059 or a quartz glass) by sputtering in an atmosphere containing oxygen. To improve productivity, A film to be deposited by decomposing a tetra-ethyl-ortho-silicate (TEOS) in plasma chemical vapor deposition (CVD) may be used.

An amorphous silicon film having a thickness of 300 to 5000 Å, preferably 500 to 1000 Å is deposited by plasma CVD and low pressure CVD (LPCVD) and then placed in a reducing atmosphere at 550 to 600 °C for 4 to 48 hours to crystallize it. After this process, crystallinity may be increased (improved) by laser irradiation. The crystallized silicon film is patterned to form island regions 1 and 2. Further, a silicon oxide film 3 having a thickness of 700 to 1500 Å is formed on the island regions 1 and 2 by sputtering.

An aluminum (containing Si of 1 weight % or Sc (scandium)

of 0.1 to 0.3 weight %) film having a thickness of 1000 Å to 3 μm is formed by electron beam evaporation or sputtering. A photoresist (for example, a product of Tokyo Ohka Co. Ltd. OFPR800/30cp) is formed by spin coating. When an aluminum oxide film having a thickness of 100 to 1000 Å is formed on a surface thereof by anodization after formation of the photoresist, adhesion to the photoresist is high. Also, by suppressing a leak current from a photoresist, it is effective on formation of a porous anodic oxide in only side surface in a later anodization process. The photoresist and the aluminum film are patterned and etched to form gate electrodes 4 and 5 and mask films 6 and 7. (Fig.10A)

The formed substrate is anodized by supplying a current in an electrolytic solution, to form an anodic oxide having a thickness of 3000 to 6000 Å, for example, 5000 Å. The anodization is performed using an acid solution containing citric acid, nitric acid, phosphoric acid, chromic acid, sulfuric acid, oxalic acid or the like of 3 to 20 % by applying a voltage of 10 to 30 V to a gate electrode at a constant current. In the embodiment, the anodization is performed in an oxalic acid solution (30 °C) at 10 V for 20 to 40 minutes. A thickness of an anodic oxide is adjusted by an anodization time. (Fig.10B)

After that, the mask films are removed, and then a current is supplied to the gate electrodes in an electrolytic solution (ethylene glycol solution containing tartaric acid, boric acid, nitric acid of 3 to 10 %) again. In order to obtain a superior oxide film, it is preferred that a temperature of the solution is about 10 °C and lower than a room temperature. As a result, barrier type anodic oxides 10 and 11 are formed in upper and side surfaces of the gate electrodes. Thicknesses of the anodic oxides 10 and 11 are proportional to an applied voltage. For example, when an applied voltage is 150 V, an anodic oxide having a thickness of 2000 Å is formed. Thicknesses of the

anodic oxides 10 and 11 are determined by a necessary offset size. Although an anodic oxide having a thickness of 3000 Å or more is formed by applying 250 V or higher, since this influences TFT characteristics, it is desired that an anodic oxide having a thickness of 3000 Å or less is formed. In the embodiment, a voltage is increased until 80 to 150 V and selected by necessary thicknesses of the anodic oxides 10 and 11.

In this state, although a barrier type anodic oxide is formed by a later process, the barrier type anodic oxides 10 and 11 are formed between the porous anodic oxides 8 and 9 and the gate electrodes 4 and 5 without forming barrier type anodic oxides outside porous anodic oxides.

An insulating film 3 is etched by dry etching or wet etching. A depth of etching is arbitrary. Etching may be performed until an active layer formed under the insulating film 3 is exposed. Etching may be stopped on halfway. However, it is desired to etch the insulating film 3 until an active layer is exposed, in mass productivity, yield and uniformity. In this state, insulating films 12 and 13 covered with the anodic oxides 8 and 9 and the gate electrodes 4 and 5 remain as a gate insulating film. (Fig.10C)

After that, the anodic oxides 8 and 9 are removed. it is preferred that a solution containing phosphoric acid, for example, a mixture acid containing phosphoric acid, acetic acid and nitric acid is used as an etchant. In using an etchant containing phosphoric acid, an etching rate of a porous anodic oxide is ten times or more as large as that of a barrier type anodic oxide. Therefore, since barrier type anodic oxides 10 and 11 are not etched substantially by the etchant containing phosphoric acid, the gate electrodes can be protected from etching.

In such structure, a source and a drain are formed by implanting N-type or P-type impurity ion into an active layer.

In a state wherein a left TFT region is covered with a mask 14, a phosphorus ion is irradiated (introduced) by ion doping at a relatively low speed (an accelerating voltage of 5 to 30 kV, 20 kV in the embodiment). A doping gas is phosphine (PH_3). A dose is 5×10^{14} to 5×10^{15} cm^{-2}. In this process, since a phosphorus ion cannot be transmitted through the insulating film 13, it is implanted into only region in which a surface is exposed, so that a drain 15 and a source 16 of an N-channel type TFT are formed. (Fig.10D)

Also, a phosphorus ion is irradiated by ion doping at a relatively high speed (an accelerating voltage of 60 to 120 kV, 90 kV in the embodiment). A dose is 1×10^{13} to 5×10^{14} cm^{-2}. In this process, a phosphorus ion is transmitted through the insulating film 13 and reaches a region formed under the film 13. However, since a dose is small, N-type regions 17 and 18 each having a low concentration are formed. (Fig.10E)

After phosphorus doping, the mask is removed. Then, using the N-channel type TFT as a mask, as described above, a source 19, a drain 20 and a P-type regions 21 and 22 each having a low concentration in a P-channel type TFT. A KrF excimer laser (wavelength of 248 nm and pulse width of 20 ns) is irradiated to activate an impurity ion introduced into an active layer.

A silicon oxide film having a thickness of 3000 to 6000 Å is formed as an interlayer insulator 23 on a whole surface by CVD. Also, contact holes are formed in a source and a drain of a TFT and then aluminum wiring-electrodes 24 to 26 are formed. Further, hydrogen annealing is performed at 200 to 400 °C. As a result, a complementary invertor circuit using TFTs is completed. (Fig.10F)

A shift register in the embodiment is formed in a basis of the above complementary invertor circuit. A shift register used in a driver circuit of an active matrix type display device and an active matrix circuit having pixel TFTs are formed on the same substrate.

Referring with Fig.3, an embodiment of the present invention will be described.

In the embodiment, one main register line and one subregister line are used in each register group, and three registers are included in each register line. Also, the number of register groups is a positive integer and a multiple of three, for example.

As shown in Fig.3, a shift register circuit 135 includes register groups 130a, ..., 130b. The register group 130a includes a main register line 131a having registers SRM_1, SRM_2 and SRM_3 and a subregister line 131b having registers SRS_1, SRS_2 and SRS_3. The register group 130b includes a main register line 131c having registers SRM_{N-2}, SRM_{N-1} and SRM_N and a subregister line 131d having registers SRS_{N-2}, SRS_{N-1} and SRS_N.

Register line selecting switches 133a and 133b are arranged to select the register lines in each register group. Defect detection terminals 134a and 134b are arranged to detect outputs of last registers of the register lines, so that whether or not each register line includes defect is detected.

Register column selecting switches 132a to 132f are arranged to select registers included in the selected register lines in each register group.

First, the main register line is examined by using the defect detection terminal in each register group. If the line is normal, the register line selecting switch is connected with the main register line. On the other hand, if the main register line has defect, the register line selecting switch is connected with the subregister line.

A conventional shift register circuit is compared with a shift register circuit according to the present invention.

In a conventional shift register circuit as shown in Fig.2, when a defective rate per register is f_n($0 < f_n < 1$) and the number of registers to be serial-connected is N (a positive

integer and a multiple of three), a probability An which a conventional shift register circuit as shown in Fig.2 is operated normally is obtained by the following equation,

$$An = (1 - f_n)^N.$$

In a shift register circuit of the present invention, the same defective rate per register f_n($0 < f_n < 1$) is used. Also, the number of registers when all registers of each register group in one line are connected in serial is used as N (a positive integer and a multiple of three). Further, each register line includes three registers.

In this state, a probability Bn which one register group is not operated normally is obtained by the following equation,

$$Bn = \{ 1 - (1 - f_n)^3 \}^2.$$

Therefore, since the number of register groups is N/3, a probability Cn which a whole shift register circuit is operated normally is obtained by the following equation,

$$Cn = [1 - \{ 1 - (1 - f_n)^3 \}^2]^{N/3}$$

$$= [1 - \{ 1 - 2 (1 - f_n)^3 + (1 - f_n)^6 \}]^{N/3}$$

$$= [(1 - f_n)3 \{ 2 - (1 - f_n)3 \}]^{N/3}$$

If $F_n = 1 - f_n$ and $r = N/3$ (r is a positive integer),

$An = F_n^{3r}$, and

$Cn = F_n^{3r} (2 - F_n^3)^r$.

In this state, from $0 < f_n < 1$,

$0 < (1 - f_n) = F_n < 1$, and

$0 < F_n^3 < 1$.

Therefore,

$1 < (2 - F_n^3) < 2$, and

$1 < (2 - F_n^3)^r < 2^r$.

From the above relationship,

$Cn - An = F_n^{3r} \{ (2 - F_n^3)^r - 1 \} > 0$.

As a result, $An < Cn$.

When the number of registers included in a source driver

circuit is 480 and a defective rate of register is 0.001, a probability An' which a conventional source driver circuit is operated normally is

$$An' = (1 - 0.001)^{480} = 0.619.$$

On the other hand, a probability Cn' which a redundancy source driver circuit according to the present invention is operated normally is

$$Cn' = [1 - \{ 1 - (1 - 0.001)^{3} \}^{2}]^{480/3} = 0.999.$$

Therefore, it is confirmed that An' < Cn'.

As described above, redundancy of a register line increases a probability which a shift register is operated normally. If a defective rate per register is the same, this relationship is always obtained without depending on the number of registers included in one register line, the number of register lines and the number of register groups.

Structures of a register line selecting switch will be described below using Figs.11A and 11B.

The register line selecting switch includes bias circuit 90a to 90g, a priority encoder circuit 81 and a multiplexer circuit 82.

Output terminals of register lines 80a to 80h are connected with input terminals (X) of the multiplexer 82. The bias circuits are arranged in correspondent to register lines each having an output terminal, and the output terminals are connected with input terminals (X) of the priority encoder circuit 81.

When outputs of the bias circuits are held, the priority encoder circuit 81 converts a bit position of L of bit string to be input into binary data and then outputs the binary data (bit string) form output terminals (Y) to input signal selecting terminals (S) of the multiplexer circuit 82 and input signal selecting terminals (S) of a multiplexer circuit 83 used as a register column selecting switch through invertor circuits.

As described above, one of the register lines is selected using a register line selecting switch constructed by a combination of the priority encoder circuit 81, the multiplexer circuit 82 and the bias circuits 90a to 90g.

Fig.7A shows an equivalent circuit of a 8 bit priority encoder circuit, and Fig.7B shows an equivalent circuit of a 8 bit input multiplexer circuit. Also, Fig.12 shows a truth table of the priority encoder circuit of Fig.7A.

Fig.4 shows a case wherein two register lines 140a and 140b are used in one register group. Since the number of register lines is 2, it is not necessary to use a priority encoder circuit as described above. Therefore, outputs of all register lines 140a and 140b are connected with input terminals (X) of a multiplexer circuit 141 for register line selection. An output terminal of a bias circuit 144 is connected with an input signal selecting terminal (S) of the multiplexer circuit 141. Defect detection terminals 143a and 143b are used to detect a register line having defect.

When one of register line is normal, a low level (L) bias is supplied to the bias circuit 144 corresponding to the one of the register lines. Therefore, since a level of the input signal selecting terminal (S) of the multiplexer circuit 141 is determined, the multiplexer circuit 141 selects a normal register line, to use an output of a last register of the selected register line as an output of a register group having the selected register line.

A structure of a register column selecting switch will be described below using Fig.4.

Register column selecting switches includes multiplexer circuits 142a, ..., and 142b, respectively. Outputs of the registers SR_1 (SR_n) constructing each column are connected with input terminals (X) of the multiplexer circuits 142a (142b) for register column selection. To select a register in a column, an output of the bias circuit 144 is connected with input

signal selecting terminals (s) of the multiplexer circuits 142a and 142b.

As described above, a register column selecting switch is constructed by a combination of the bias circuit 144 and the multiplexer circuits 142a and 142b.

A structure of a bias circuit will be described using Figs.8A to 8C.

In a bias circuit as shown in Fig.8A, a pull-up resistor is connected with a pull-down resistor in serial, and an output terminal and a cutting portion are provided between these resistors. A resistance value ratio between the pull-up resistor and the pull-down resistor is 100 : 1, and may be set in a range which a voltage level detected on the output terminal becomes a low level (L).

A bias circuit corresponding to a normal register line holds a low level (L), and bias circuits corresponding to register lines other than the normal register line holds a high level (H) by cutting a cutting portion of the bias circuit using a laser to obtain a pull-up state. As a result, an input signal of the multiplexer circuit can be selected.

In a bias circuit as shown in Fig.8B, an analog switch using an N-type TFT is used. As described above, a bias circuit corresponding to a normal register line holds a low level (L), and bias circuits corresponding to register lines other than the normal register line holds a high level (H) by cutting a cutting portion of the bias circuit using a laser to obtain a pull-up state. As a result, an input signal of the multiplexer circuit can be selected.

Fig.8C shows cutting of a cutting portion of a bias circuit. The cutting portion may be cut by applying a high voltage to two foot prints.

As shown in Figs.11A and 11B, in a case wherein the number of register lines is n (n > 2), outputs of last registers of all register lines 80a to 80n are connect with input terminals

(X) of a multiplexer circuit 82 for register line selection. Also, bias circuits 90a to 90g each having output terminals are arranged in correspondence to the register lines, and the output terminals of the bias circuits 90a to 90g are connected with input terminals (X) of the priority encoder circuit 81. The output terminals of the priority encoder circuit 81 is connected with input signal selection terminals of the multiplexer circuit 82 through invertor circuits.

When a normal register line is detected, an output of a bias circuit corresponding to the register line is held to a low level (L). An output of a bias circuit corresponding to the register line is held to a low level (L). Also, an output of a bias circuit corresponding to the register line other than the normal register line is held to a high level (H). As described above, outputs of the priority encoder circuit 81 are determined by holding output levels of the output terminals of the bias circuits. Therefore, since levels of input signal selection terminals of the multiplexer circuit 82 are determined, the multiplexer circuit 82 selects a normal register line, so that an output of a last register of the selected register line is input to an input terminal of an OR circuit 84. An output of the OR circuit 84 is used as an input of next register group in a case wherein a plurality of register groups are arranged in a shift register circuit.

A register column is defined at a column direction of registers of register lines. Multiplexer circuits for register column selection are arranged for each register column. The number of the multiplexer circuits for register column selection coincide with the number of registers of one register line.

When a normal register line is selected in one register group, an output of the priority encoder circuit 81 is input to input signal selection terminals (S) of a multiplexer circuit 83 for register column selection through invertor circuits.

Therefore, registers included in the selected register line are selected in a column direction, so that sample timing signals can be output to source lines of an active matrix type display device.

Fig.13 shows a case wherein two register lines 140a and 140b are used in one register group and a shift register circuit has only one register group. As shown in Fig.13, a multiplexer circuit for register line selection can be omitted in comparison with Fig.4.

As described above, a normal register line is selected in each register group, and a shift register circuit is constructed by connecting with each register group each other.

In the above embodiment, although a complementary type is used, a circuit using an N-channel type or a P-channel type may be constructed. In this state, since only one impurity doping process is performed, the number of forming processes can be decreased. Figs.9A to 9C show shift register circuit constructed by only P-channel type. Fig.9A shows an invertor circuit constructed using P-channel transistors and resistors. Fig.9B shows an invertor circuit constructed using P-channel transistors. Fig.9C shows a dynamic type shift register. A multiplexer circuit, a priority encoder circuit and like can be constructed using P-channel transistors and resistors.

In the embodiment, although only P-channel type transistor is used, a N-channel type transistor can be used.

According to the present invention, a defective rate of one register is constant and redundancy shift register circuit is used, so that a yield of a whole shift register circuit can be increased and reliability of a shift register circuit can be improved.

WHAT IS CLAIMED IS:

1. An active matrix type display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a driver circuit comprising a plurality of thin film transistors for driving said plurality of switching elements,

wherein each of said plurality of thin film transistors comprises a crystalline semiconductor layer, a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film.

2. The active matrix type display device according to claim 1 wherein said gate electrode is located over said semiconductor layer.

3. The active matrix type display device according to claim 1 wherein all of said plurality of thin film transistors are p-type.

4. The active matrix type display device according to claim 1 wherein all of said plurality of thin film transistors are n-type.

5. The active matrix type display device according to claim 1 wherein said substrate is a glass substrate.

6. The active matrix display device according to claim 1 wherein said crystalline semiconductor layer comprises silicon.

7. An active matrix type display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a driver circuit comprising a plurality of thin film transistors for driving said plurality of switching elements, wherein each of said plurality of thin film transistors comprises a crystalline semiconductor layer, a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film,

wherein said crystalline semiconductor layer has source and drain regions and at least one lightly doped region.

8. The active matrix type display device according to claim 7 wherein said substrate is a glass substrate.

9. The active matrix type display device according to claim 7 wherein said source and drain regions and said at least one lightly doped region are doped with phosphorus.

10. The active matrix type display device according to claim 7 wherein said source and drain regions and said at least one lightly doped region are doped with boron.

11. The active matrix type display device according to claim 7 wherein said gate electrode is located over said semiconductor layer.

12. The active matrix display device according to claim 7 wherein said crystalline semiconductor layer comprises silicon.

13. An active matrix type display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a CMOS circuit comprising at least one n-channel type thin film transistor and one p-channel type thin film transistor,

wherein each of said n-channel and p-channel type thin film transistors comprises a crystalline semiconductor layer, a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film.

14. The active matrix type display device according to claim 13 wherein said substrate is a glass substrate.

15. The active matrix type display device according to claim 13 wherein said gate electrode is located over said semiconductor layer.

16. The active matrix display device according to claim 13 wherein said crystalline semiconductor layer comprises silicon.

17. An active matrix type display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a CMOS circuit comprising at least one n-channel type thin film transistor and one p-channel type thin film transistor, each of said thin film transistors comprising a crystalline semiconductor layer, a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film,

wherein said crystalline semiconductor layer has source and drain regions and at least one lightly doped region.

18. The active matrix type display device according to claim 17 wherein said substrate is a glass substrate.

19. An active matrix type display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a driver circuit comprising a plurality of thin film transistors for driving said plurality of switching elements,

wherein each of the film transistors of said switching elements and said driver circuit comprises a crystalline semiconductor layer, a gate insulating film

adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film.

20. The active matrix type display device according to claim 19 wherein said gate electrode is located over said semiconductor layer.

21. The active matrix type display device according to claim 19 wherein all of said plurality of thin film transistors are p-type.

22. The active matrix type display device according to claim 19 wherein all of said plurality of thin film transistors are n-type.

23. The active matrix type display device according to claim 19 wherein said substrate is a glass substrate.

24. The active matrix display device according to claim 19 wherein said crystalline semiconductor layer comprises silicon.

25. An active matrix type display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a driver circuit comprising a plurality of thin film transistors for driving said plurality of switching elements,

wherein each of the thin film transistors of the switching elements and the driver circuit comprises a crystalline semiconductor layer, a gate insulating

film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film,

wherein said crystalline semiconductor layer has source and drain regions and at least one lightly doped region.

26. The active matrix type display device according to claim 25 wherein said substrate is a glass substrate.

27. The active matrix type display device according to claim 25 wherein said source and drain regions and said at least one lightly doped region are doped with phosphorus.

28. The active matrix type display device according to claim 25 wherein said source and drain regions and said at least one lightly doped region are doped with boron.

29. The active matrix type display device according to claim 25 wherein said gate electrode is located over said semiconductor layer.

30. The active matrix display device according to claim 25 wherein said crystalline semiconductor layer comprises silicon.

31. An active matrix type display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a CMOS circuit comprising at least one n-channel type thin film transistor and one p-channel type thin film transistor,

wherein each of the film transistors of the switching elements and said n-channel and p-channel type thin film transistors comprises a crystalline semiconductor layer, a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film.

32. The active matrix type display device according to claim 31 wherein said substrate is a glass substrate.

33. The active matrix type display device according to claim 31 wherein said gate electrode is located over said semiconductor layer.

34. The active matrix display device according to claim 31 wherein said crystalline semiconductor layer comprises silicon.

35. An active matrix type display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a CMOS circuit comprising at least one n-channel type thin film transistor and one p-channel type thin film transistor,

wherein each of the film transistors of the switching elements and said n-channel and p-channel type thin film transistors comprises a crystalline semiconductor layer, a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film, and said crystalline

semiconductor layer has source and drain regions and at least one lightly doped region.

36. The active matrix type display device according to claim 35 wherein said substrate is a glass substrate.

37. The active matrix display device according to claim 35 wherein said crystalline semiconductor layer comprises silicon.

38. The active matrix display device according to claim 17 wherein said crystalline semiconductor layer comprises silicon.

Abstract of the disclosure

In a shift register circuit included in a driver circuit for driving an active matrix circuit in an active matrix type display device, a plurality of serial-connected registers constructing register lines are arranged to construct a redundancy shift register circuit. Whether or not each register line has defect is examined by detecting an output of a last register of each register line. When the register line having defect is detected by the examination, a normal register line is selected by a shift register selecting switch, and the serial-connected registers of the selected register line are used in the shift register circuit.

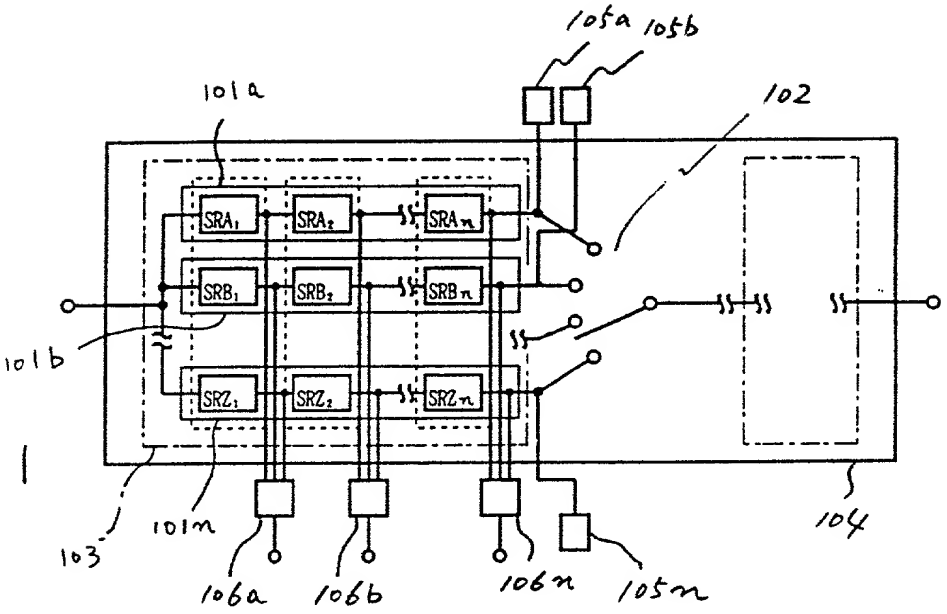


FIG. 1

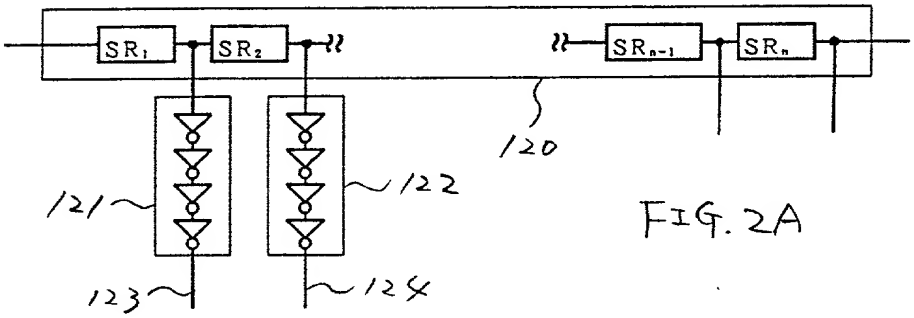


FIG. 2A

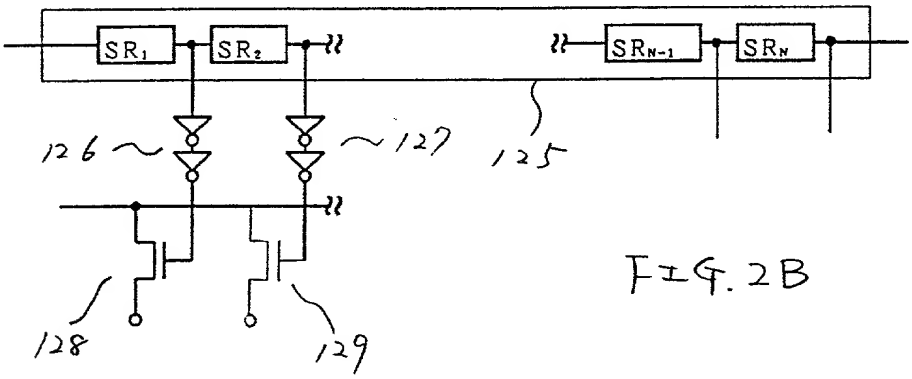


FIG. 2B

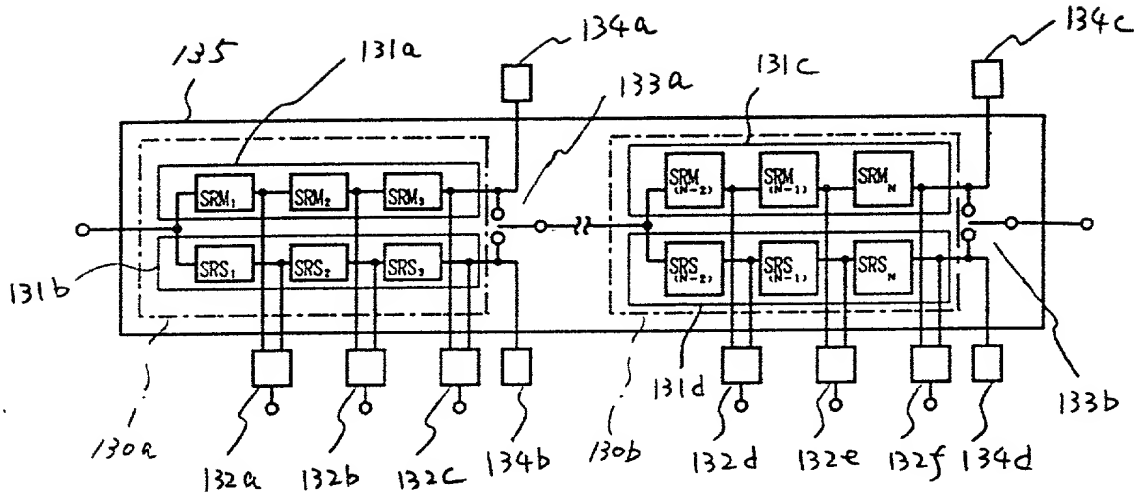

135
131a
134a
133a
131c
134c
131b
130a
132a
132b
132c
134b
130b
131d
132d
132e
132f
134d
133b

FIG. 3

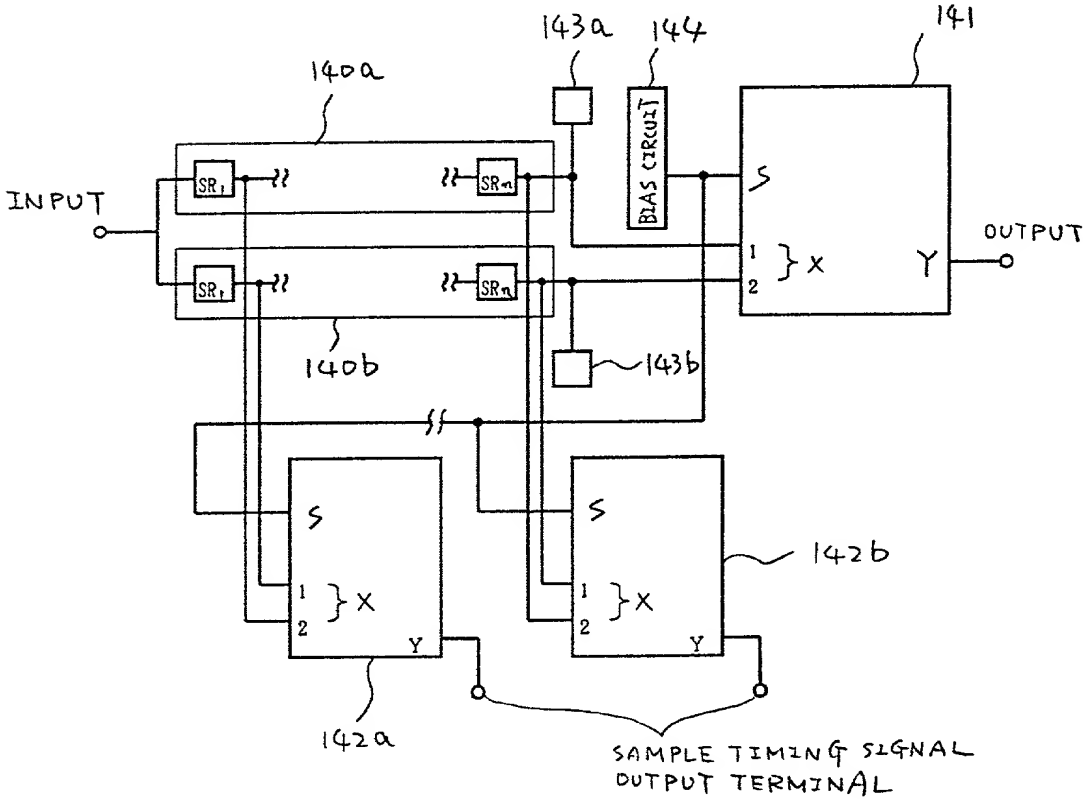

143a
144
141
140a
INPUT
BIAS CIRCUIT
OUTPUT
140b
143b
142b
142a
SAMPLE TIMING SIGNAL
OUTPUT TERMINAL

FIG. 4

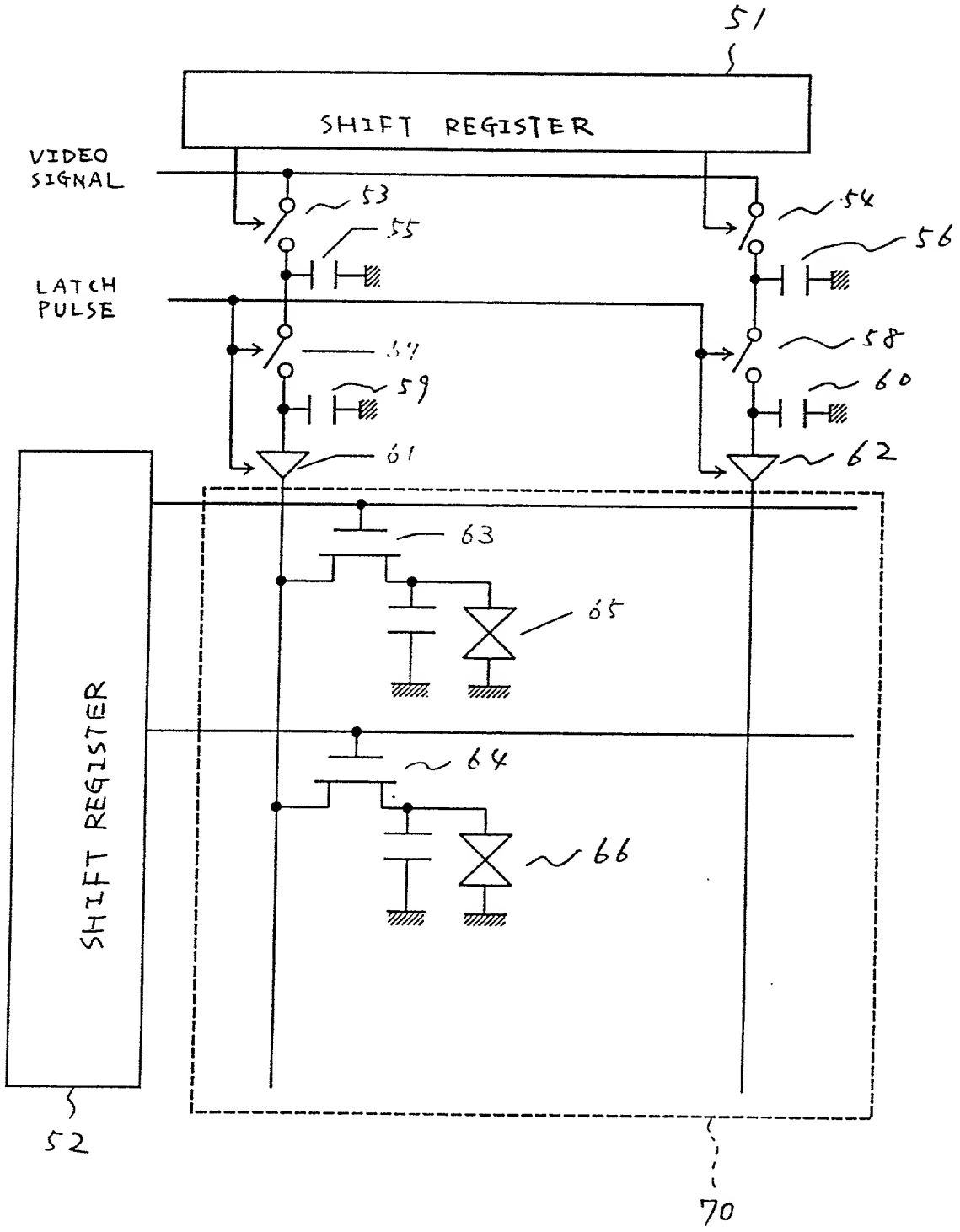

51
SHIFT REGISTER
VIDEO SIGNAL
53
54
55
56
LATCH PULSE
57
58
59
60
61
62
63
65
64
66
SHIFT REGISTER
52
70

FIG. 5

Fig 6A

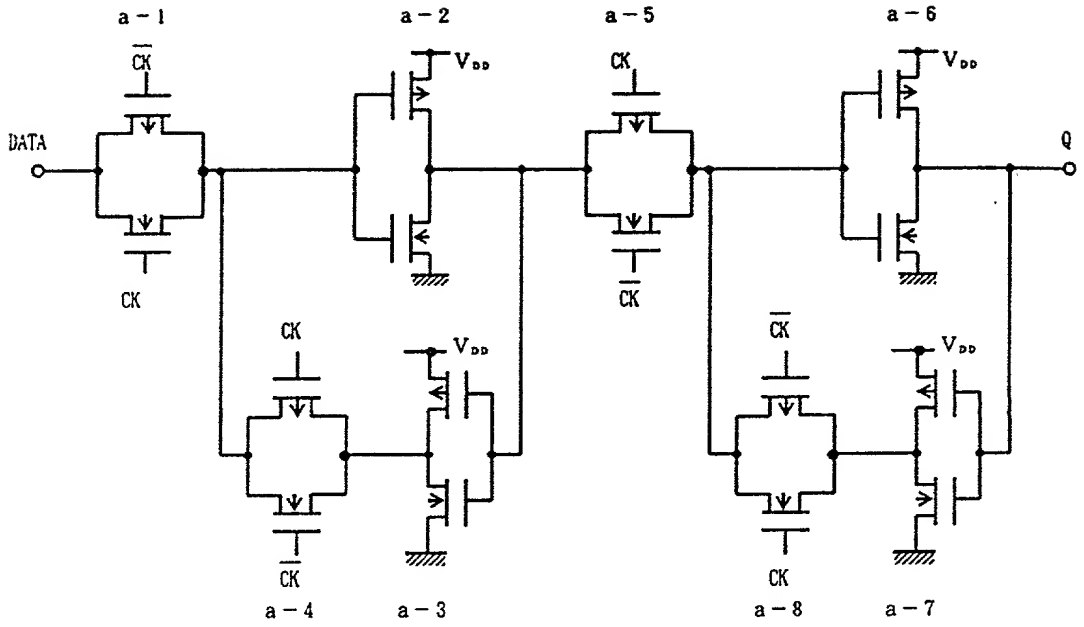

a-1
a-2
a-5
a-6
DATA
Q
CK
$\overline{CK}$
V_{DD}
a-4
a-3
a-8
a-7

Fig 6B

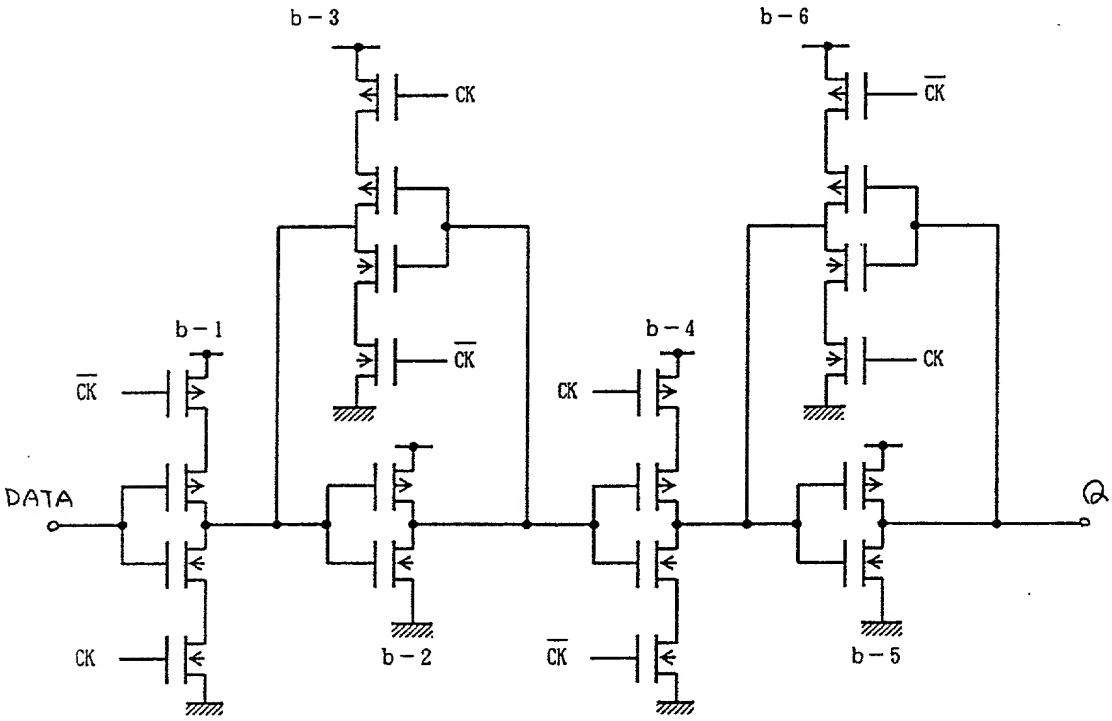

b-3
b-6
b-1
b-4
b-2
b-5
DATA
Q
CK
$\overline{CK}$

Fig 7A

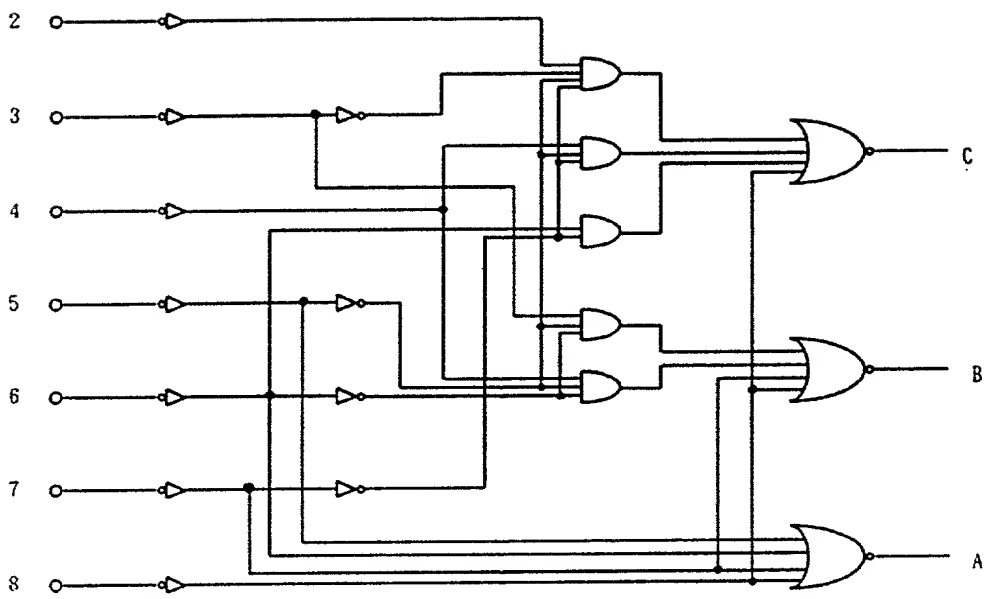
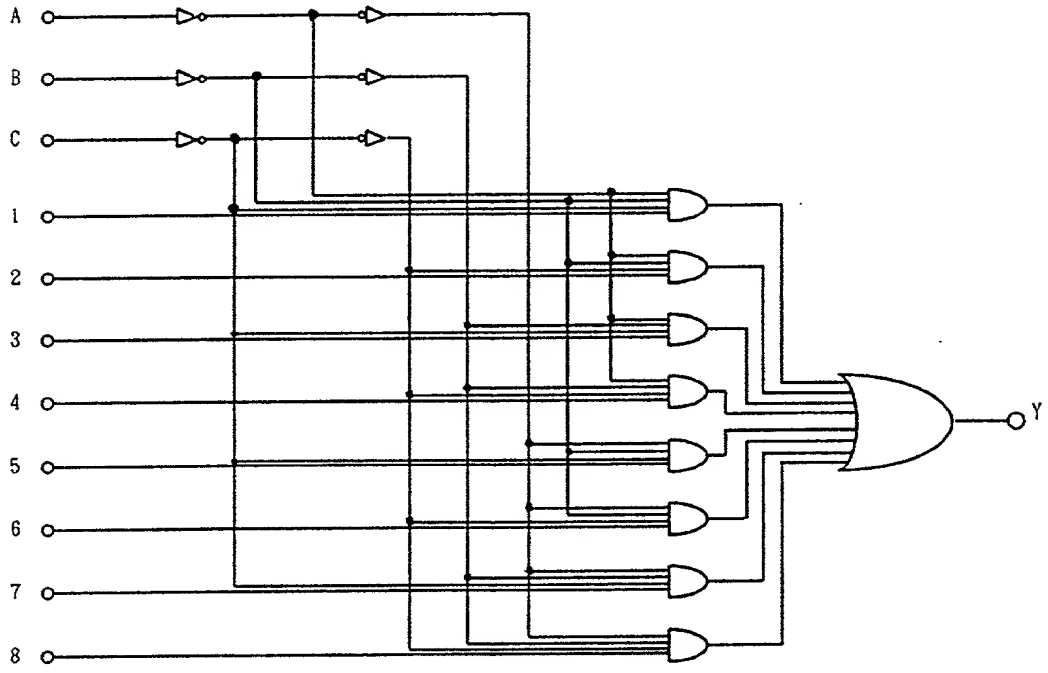


Fig 7B



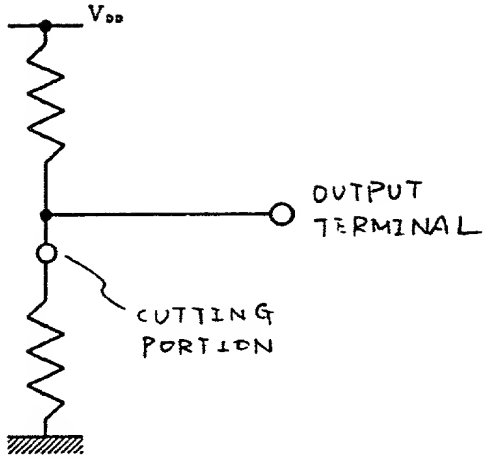


FIG. 8A

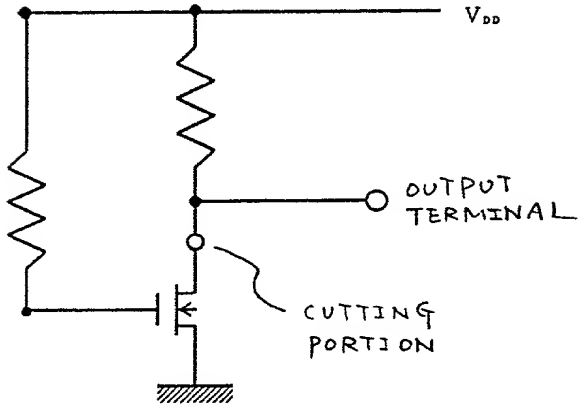


FIG. 8B

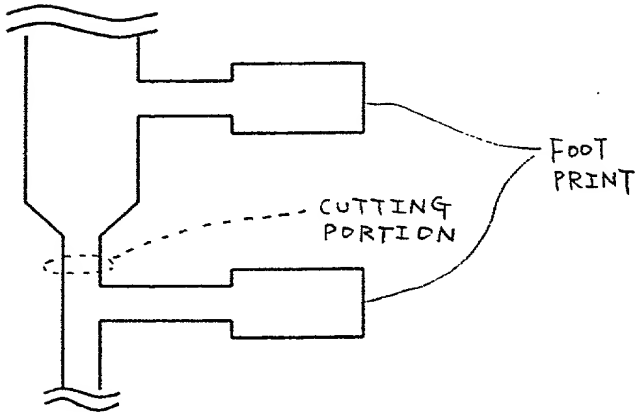


FIG. 8C

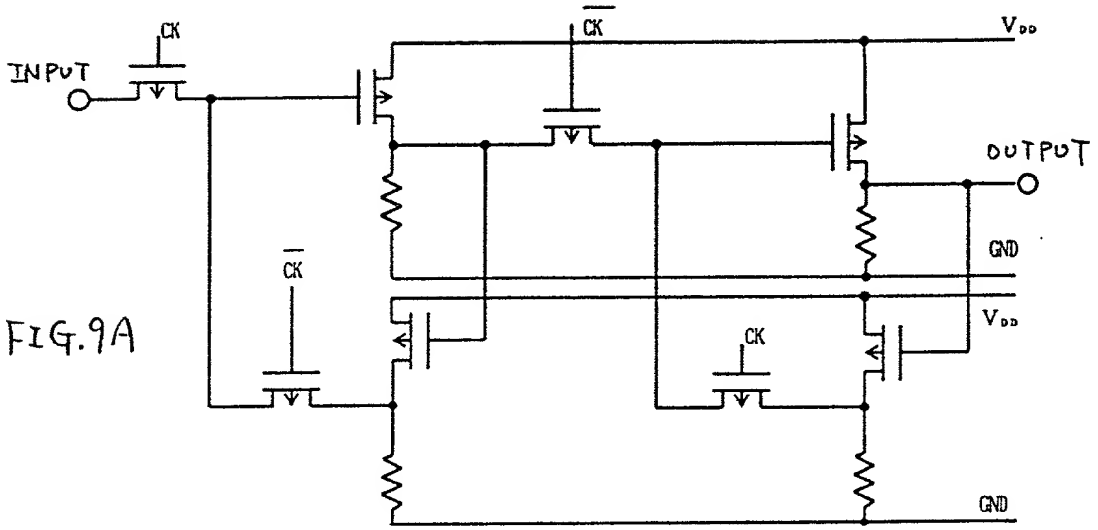


FIG.9A

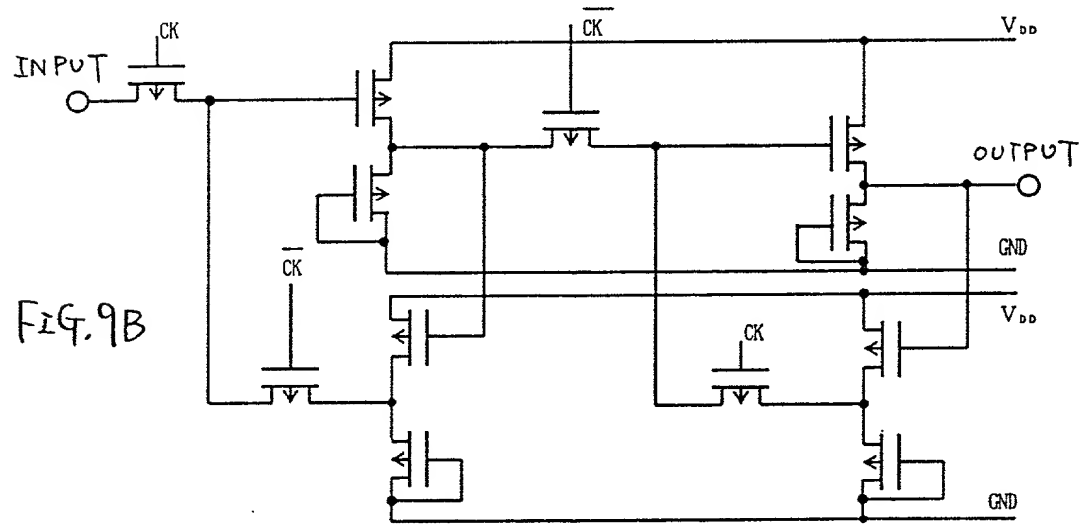


FIG.9B

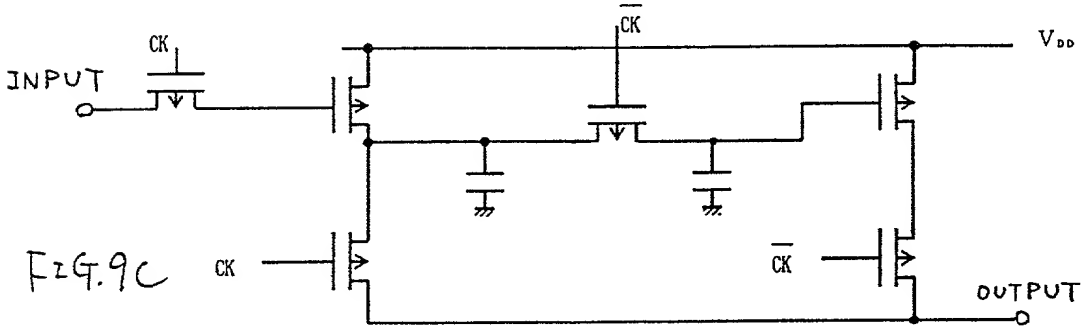


FIG.9C

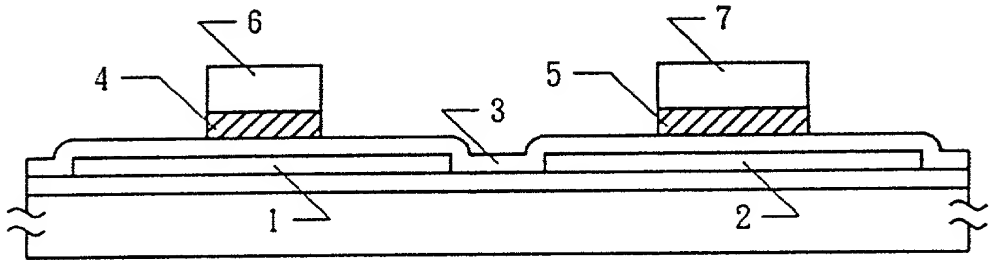


Fig 10A

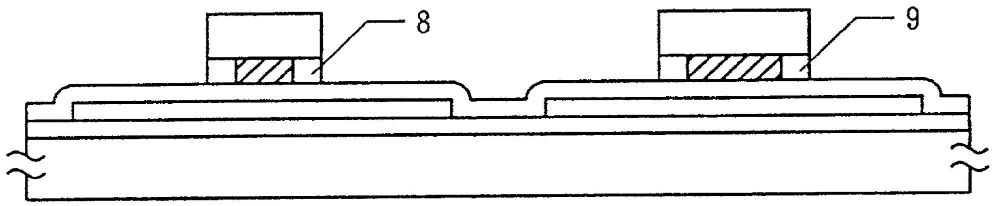


Fig 10B

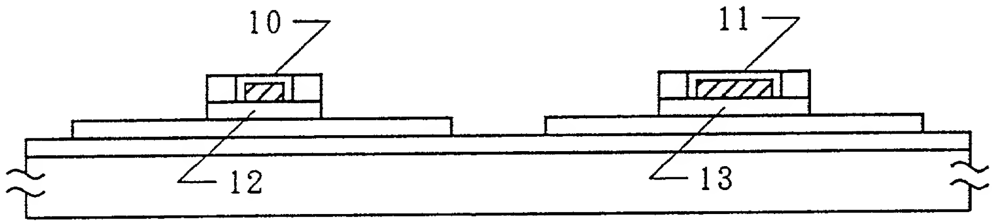


Fig 10C

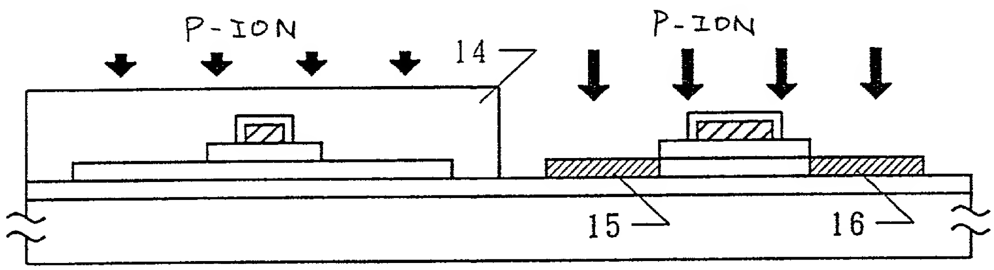


Fig 10D

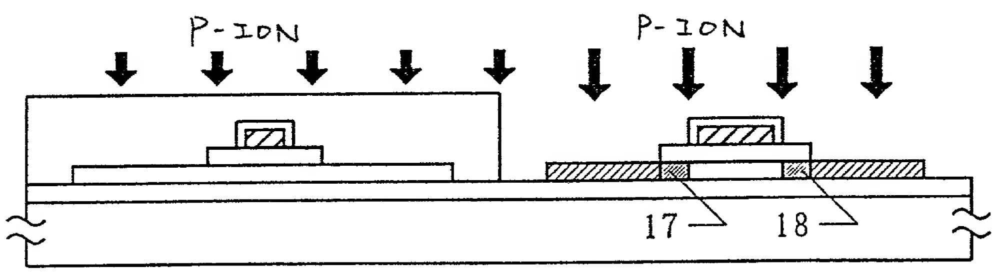


Fig 10E

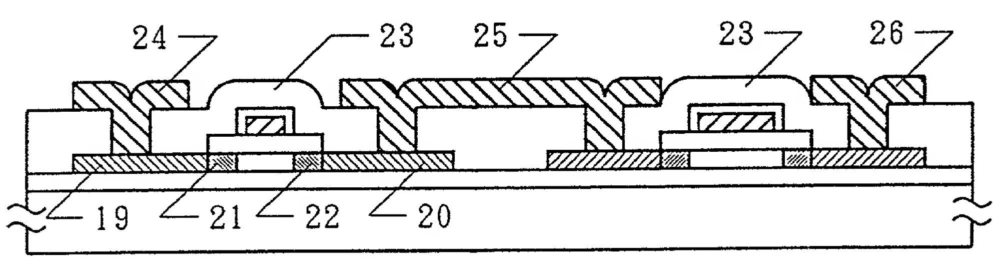


Fig 10F

FIG. 11B

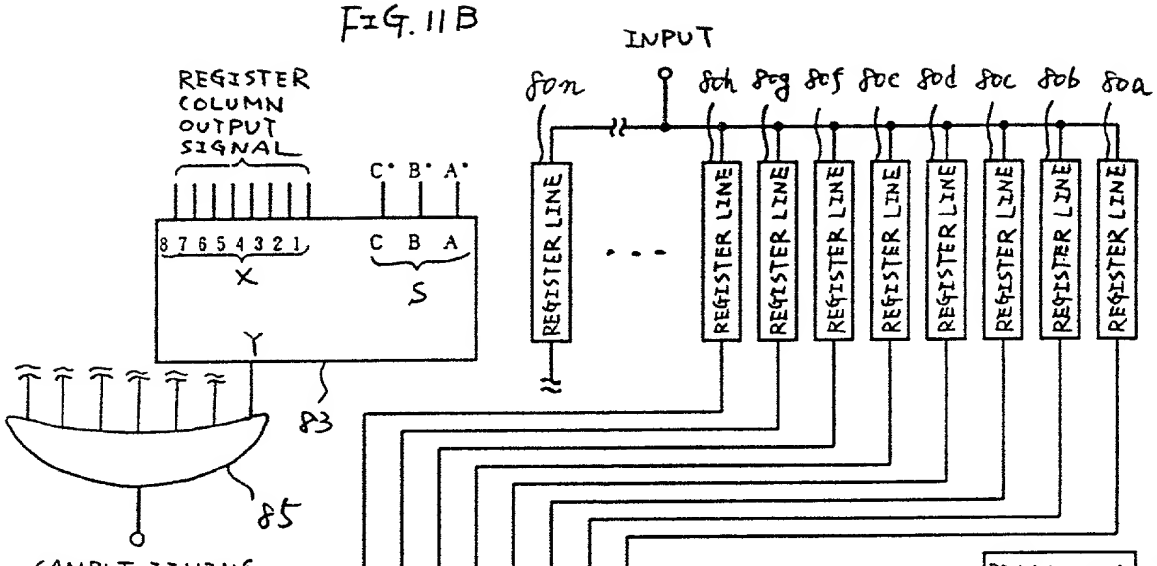
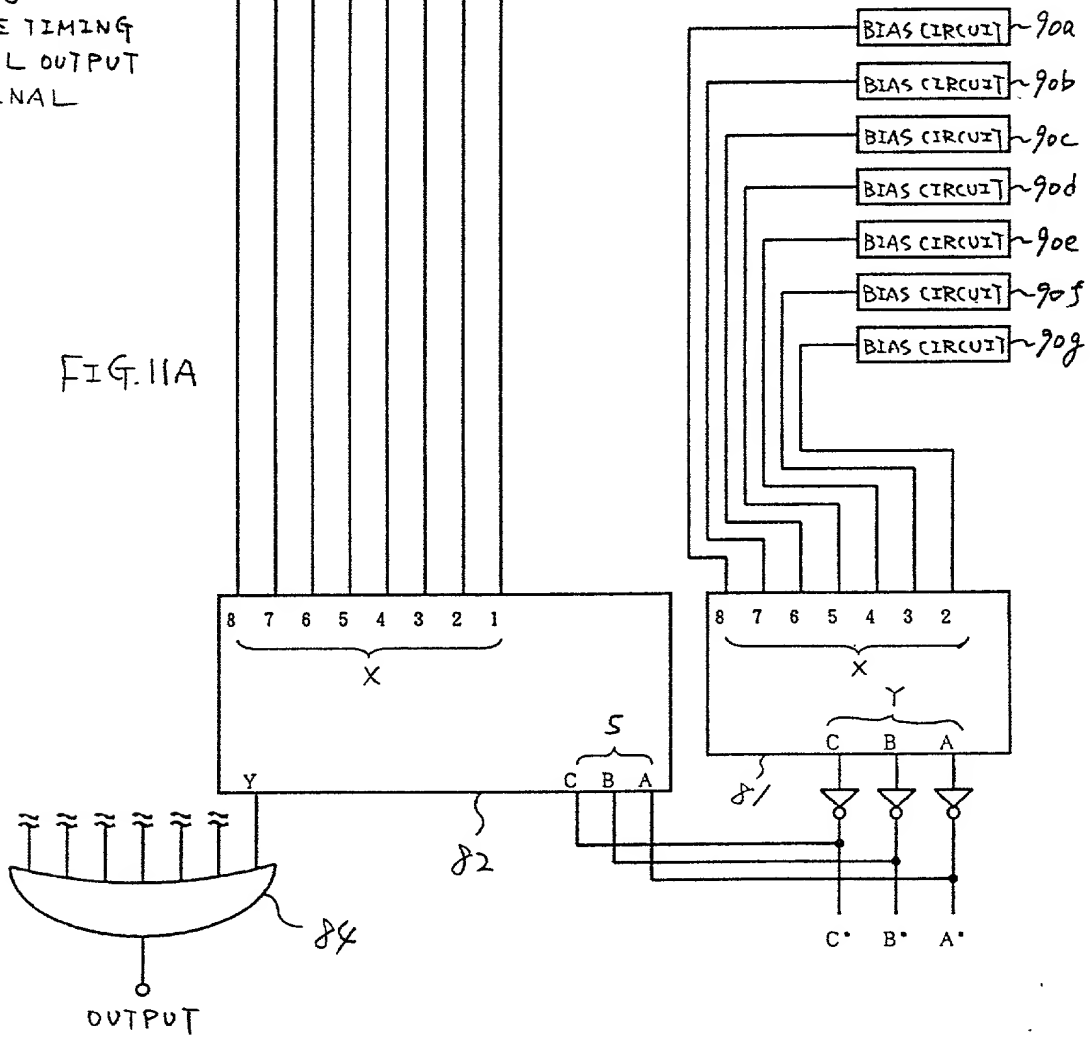


FIG. 11A



INPUT							OUTPUT		
2	3	4	5	6	7	8	A	B	C
H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	L
*	L	H	H	H	H	H	H	L	H
*	*	L	H	H	H	H	H	L	L
*	*	*	L	H	H	H	L	H	H
*	*	*	*	L	H	H	L	H	L
*	*	*	*	*	L	H	L	L	H
*	*	*	*	*	*	L	L	L	L

*:don' t care

FIG. 12

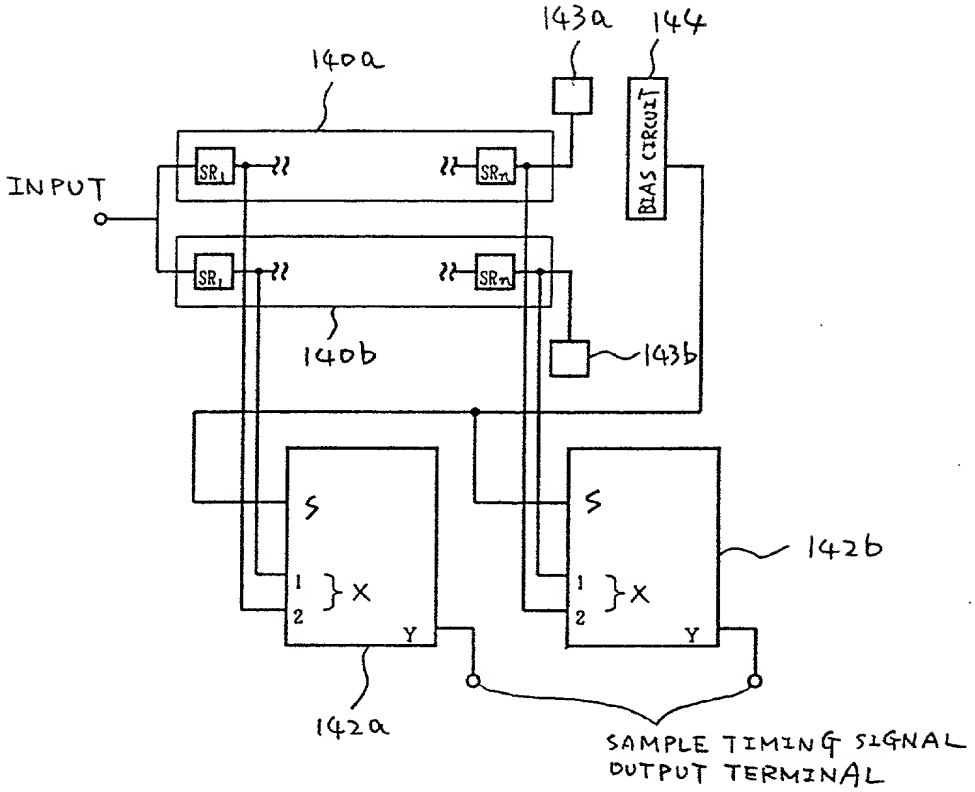

143a
144
140a
INPUT
SR1
SRn
BIAS CIRCUIT
140b
143b
S
1
2
X
Y
142b
142a
SAMPLE TIMING SIGNAL
OUTPUT TERMINAL

FIG. 13

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO.
0756-1243

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: * REDUNDANCY SHIFT REGISTER CIRCUIT FOR DRIVER CIRCUIT IN ACTIVE MATRIX TYPE LIQUID CRYSTAL DISPLAY DEVIC, the specification of which is attached hereto unless the following box is checked:

Insert Title

Check Box If Appropriate — For Use Without Specification Attached

☒ The specification was filed on April 21, 1995
and was assigned Serial No. 08/427,096 (if known)
and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Prior Foreign Application(s)

Insert Priority Information (if appropriate)

(Number)	(Country)	(Month/Day/Year Filed)	Priority Claimed	
6-107574	JAPAN	April 22, 1994	☒ Yes	☐ No
			☐ Yes	☐ No
			☐ Yes	☐ No
			☐ Yes	☐ No
			☐ Yes	☐ No

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months Prior To The Filing Date of This Application:

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status—patented, pending, abandoned)

I hereby appoint the following attorneys to prosecute this application and/or any international application and to transact all business in the Patent and Trademark Office connected therewith:

Daniel W. Sixbey (Reg. No. 20,932)	Gerald J. Ferguson, Jr. (Reg. No. 23,016)
Stuart J. Friedman (Reg. No. 24,312)	David S. Safran (Reg. No. 27,997)
Charles M. Leedom, Jr. (Reg. No. 26,477)	Thomas W. Cole (Reg. No. 28,290)

Send Correspondence to:

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING

SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
2010 Corporate Ridge, Suite 600
McLean, Virginia 22102
Telephone: (703) 790-9110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Insert Name of Non-U.S. firm, attorney or agent

The undersigned hereby authorize any U. S. attorney or agent named herein to accept and follow instructions from _____ as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U. S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

Insert Full Name of First or Sole Inventor and Date This Document Is Signed

Insert Residence Insert Citizenship

Insert Post Office Address

FULL NAME OF SOLE OR FIRST INVENTOR Jun KOYAMA	INVENTOR'S SIGNATURE Jun Koyama	DATE 6/15/1995	
RESIDENCE (City, State & Country) Kanagawa, Japan	CITIZENSHIP Japanese		
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Second Inventor: see above FULL NAME OF SECOND JOINT INVENTOR, IF ANY Yuji KAWASAKI	INVENTOR'S SIGNATURE Yuji Kawasaki	DATE 6/15/1995	
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Third Inventor: see above FULL NAME OF THIRD JOINT INVENTOR, IF ANY	INVENTOR'S SIGNATURE	DATE	
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Fourth Inventor: see above FULL NAME OF FOURTH JOINT INVENTOR, IF ANY	INVENTOR'S SIGNATURE	DATE	
RESIDENCE (City, State & Country)	CITIZENSHIP		
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			

Docket No. 0756-2070

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of	)
Jun KOYAMA et al.	)
Based On Serial No. 08/803,217	) Art Unit: 2775
Which Was Filed: February 20, 1997	) Examiner: P. Bell
For: REDUNDANCY SHIFT REGISTER	)
CIRCUIT FOR DRIVER CIRCUIT	)
IN ACTIVE MATRIX TYPE LIQUID	)
CRYSTAL DISPLAY DEVICE	) Date: November 24, 1999

NOTICE OF CHANGE OF ADDRESS

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231
Sir:

Effective immediately, please note that the address of the attorney(s) of record in the above-referenced application has been changed. Please direct all future correspondence to:

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